TRANSACTION ALIGNER MICROARCHITECTURE

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ABSTRACT

A computer system is provided that includes a direct memory access (DMA) controller, a memory control device and a slave device, all coupled to a system bus. The DMA controller is configured to implement fly-by read and fly-by write operations between the memory control device and the slave device. The memory control device and the slave device each include read and write aligners. During a fly-by read, data is read from slave device and aligned to the system bus using a peripheral read aligner. The memory control device re-aligns the data received on the system bus using a write aligner and writes the data to a main memory. During a fly-by write, data is read from the main memory and aligned to the system bus using a read aligner in memory control device. A write aligner in the slave device then re-aligns the data received on the system bus.

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